



501.36127CC3

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: KOUBUCHI et al

Serial No.: 10/619,039

Filed: July 14, 2003

For: Semiconductor Integrated Circuit Device

Art Unit: 2814

Examiner: L. Pham

CITATION OF DOCUMENTS UNDER 37 CFR 1.56

Mail Stop: DD  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

October 21, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith, under 37 CFR 1.56, a copy of United States Patent No. 5,614,445 to Hirabayashi.

This patent discloses a method of dicing a semiconductor wafer, including forming trench grooves in the integrated circuit region of the wafer and dummy etched grooves in a scribe line zone of the wafer. Both the trench grooves and the dummy etched grooves are filled with polycrystalline silicon to provide a smooth wafer surface. This patent discloses forming a sidewall insulating film 8 on the inner sidewall of the trench, as shown in Figure 3 and as described at column 5, lines 56 - 64, and describes the etching problem at column 3, lines 26 - 44.

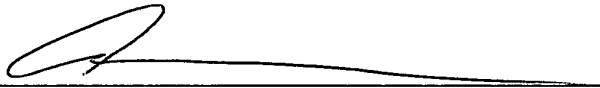
However, the document does not disclose the dishing problem of the polishing method, and does not disclose an insulating film buried in the trench by polishing an insulating film formed over the trench.

Consideration of the Hirabayashi patent by the Examiner is requested.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (Case: 501.36127CC3), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

A handwritten signature in black ink, consisting of a large, stylized 'A' followed by a horizontal line that tapers to the right.

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Attachments

